NITRIDE SEMICONDUCTOR AND FABRICATION METHOD THEREOF

Technical Field

The present invention relates to nitride semiconductor, and more particularly, to GaN-based nitride semiconductor and fabrication method thereof.

Background Art

Generally, a GaN-based nitride semiconductor is applied to electronic devices that are high-speed switching and high power devices such as optic elements of blue/green LEDs, MESFET, HEMT, etc. In particular, the blue/green LED is under a state in which mass-production has been already progressed and a global sale is being exponentially increased.

Such a GaN-based nitride semiconductor is grown up usually on a sapphire or SiC substrate. At a low growth temperature, a polycrystalline layer of $Al_xGa_{1-x}N$ is grown as a buffer layer on a sapphire substrate or a SiC substrate. After that, at a high temperature, a good quality GaN-based single crystalline layer is grown on the buffer layer, thereby fabricating the GaN-based nitride semiconductor.

Meanwhile, to improve the performance of the GaN-based nitride semiconductor and assure the reliability thereof, an innovative buffer layer is researched and the GaN-based nitride semiconductor fabrication method has been studied very actively.

Disclosure of the Invention

An object of the present invention is to provide a nitride semiconductor and fabrication method thereof that can reduce crystal defects caused by a differences between thermal expansion coefficients of a GaN-based

single crystalline layer and a substrate and a difference between lattice constants of them and enhance the crystallinity of the GaN-based nitride semiconductor, to thereby improve the performance of the nitride semiconductor and assure reliability.

Another object of the present invention is to provide a nitride semiconductor light emitting device (LED) that can improve the performance thereof and assure the reliability.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, a nitride semiconductor includes: a substrate; a GaN-based buffer layer formed on the substrate in any one selected from a group consisting of a three-layered structure $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$, a two-layered structure $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$; and a GaN-based single crystalline layer formed on the GaN-based buffer layer.

In an aspect of the present invention, there is provided a method for fabricating a nitride semiconductor. The method includes the steps of: (a) growing a GaN-based buffer layer on a substrate in any one selected from a group consisting of a three-layered structure $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$, a two-layered structure $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$; and (b) growing a GaN-based single crystalline layer on the grown GaN-based buffer layer.

In another aspect of the present invention, a nitride semiconductor light emitting device includes: a substrate; a GaN-based buffer layer formed on the substrate in any one selected from a group consisting of

a three-layered structure $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$, a two-layered structure $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$; a first electrode layer of an n-GaN layer formed on the GaN-based buffer layer; an activation layer formed on the first electrode layer; and a second electrode layer of a p-GaN layer formed on the activation layer.

Brief Description of the Drawings

FIGs. 1(a) and 1(b) are schematic diagrams illustrating the structure of a first embodiment of a nitride semiconductor formed by a nitride semiconductor fabrication method according to the present invention;

FIGs. 2(a) and 2(b) are schematic diagrams illustrating the structure of a second embodiment of a nitride semiconductor formed by a nitride semiconductor fabrication method according to the present invention;

FIGs. 3(a) and 3(b) are schematic diagrams illustrating the structure of a third embodiment of a nitride semiconductor formed by a nitride semiconductor fabrication method according to the present invention; and

FIG. 4 is a cross-sectional view schematically illustrating the structure of a nitride semiconductor LED formed by a nitride semiconductor fabrication method according to the present invention.

Best Mode for Carrying Out the Invention

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

FIGs. 1(a) and 1(b) are schematic diagrams illustrating the structure of a first embodiment of a nitride semiconductor formed by a nitride semiconductor fabrication method according to the present invention.

The nitride semiconductor according to the present invention, as shown in FIG. 1(a), includes a substrate (i.e. a sapphire substrate or a SiC substrate) 101 and a GaN-based buffer layer 110 formed on the substrate 101 in three-layered structure $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ 102 - 104 where $0 \leq x \leq 1$ and $0 \leq y \leq 1$. A GaN-based single crystalline layer 120 is formed on the GaN-based buffer layer 110. Here, the GaN-based single crystalline layer 120 includes an Indium-doped GaN layer 105, an undoped GaN layer 106, and a silicon-doped n-GaN layer 107.

As shown in FIGs. 1(a) and 1(b), in the GaN-based single crystalline layer 120, after the Indium-doped GaN layer 105 is formed, the undoped GaN layer 106 may be formed on the Indium-doped GaN layer 105. Otherwise, after the undoped GaN layer 106 is formed, the Indium-doped GaN layer 105 may be formed on the undoped GaN layer 106.

The GaN-based buffer layer 110 of the nitride semiconductor is grown in an MOCVD equipment at a temperature of 500 - 800 °C and in a thickness of 50 - 800 Å. The GaN-based buffer layer 110 is grown by while supplying carrier gases of H_2 and N_2, introducing sources of TMGa, TMIn and TMAl and gas of highly pure (>99.9995 %) NH_3 at the same time. Here, the flow of the sources of TMGa, TMIn and TMAl is 5 - 300 μmol/mim, and the growing pressure is 100 - 700 torr.

The GaN-based buffer layer 110 can efficiently cancel the stress caused due to the differences between thermal expansion coefficients of the substrate 101 and the GaN-based buffer layer 110 and between lattice

constants of the substrate 101 and the GaN-based buffer layer 110 in conjunction of the $Al_yGa_{1-y}N$ layer 102 and $In_xGa_{1-x}N$ layer 103. Accordingly, it helps GaN seed grow and be combined when the GaN seed grows upwards from the GaN layer 104 positioned at the upper portion of the GaN-based buffer layer 110. The crystal defects such as dislocation generated at the boundary between the substrate 101 and the GaN-based buffer layer 110 is minimized so that good GaN-based nitride semiconductor can be obtained.

The GaN-based crystal layer 120 of the nitride semiconductor according to the present invention is grown at the temperature of 900 - 1100 °C by using the MOCVD equipment, and by supplying sources of TMGa and TMIn. The gas of SiH_4 is used as a doping source. Here, the electrode of the n-GaN layer 107 has carrier concentration of $1 \times 10^{18}/cm^3$ or more. When the sources of TMGa and TMIn is introduced, their pressure is 100 - 700 torr and their flow is 0.1 - 700 μmol/min.

Meanwhile, FIGs. 2(a) and 2(b) are schematic diagrams illustrating structure of a second embodiment of nitride semiconductor fabricated in a nitride semiconductor fabrication method according to the present invention.

The nitride semiconductor according to the present invention, as shown in FIG. 2(a), includes a substrate (i.e. a sapphire substrate or a SiC substrate) 201 and a GaN-based buffer layer 210 formed on the substrate 201 in two-layered structure $In_xGa_{1-x}N$/GaN 202 and 203 where $0 \leq x \leq 1$. A GaN-based single crystalline layer 220 is formed on the GaN-based buffer layer 210. Here, the GaN-based single crystalline layer 220 includes an Indium-doped GaN layer 204, an undoped GaN layer 205, and a silicon-doped n-GaN layer 206.

The GaN-based buffer layer 210 helps GaN seed grow and be combined when the GaN seed grows upwards from the GaN layer 203 positioned at the upper portion of the GaN-based buffer layer 210. The crystal defects such as dislocation generated at the boundary between the substrate 201 and the GaN-based buffer layer 210 is minimized so that good GaN-based nitride semiconductor can be obtained.

As shown in FIGs. 2(a) and 2(b), in the GaN-based single crystalline layer 220 laminated and formed on the GaN-based buffer layer 210, after the Indium-doped GaN layer 204 is formed, the undoped GaN layer 205 may be formed on the Indium-doped GaN layer 204. Otherwise, after the undoped GaN layer 205 is formed, the Indium-doped GaN layer 204 may be formed on the undoped GaN layer 205.

Since the nitride semiconductor having the above-mentioned structure is grown in the process similar to the fabrication method of the nitride semiconductor described in the first embodiment, the description of the fabrication method will be omitted.

Meanwhile, FIGs. 3(a) and 3(b) are schematic diagrams illustrating structure of a third embodiment of nitride semiconductor fabricated in a nitride semiconductor fabrication method according to the present invention.

The nitride semiconductor according to the present invention, as shown in FIG. 3(a), includes a substrate (i.e. a sapphire substrate or a SiC substrate) 301 and a GaN-based buffer layer formed on the substrate 301 in superlattice structure of $In_xGa_{1-x}N$/GaN layer 302 where $0 \leq x \leq 1$. A GaN-based single crystalline layer 320 is formed on the $In_xGa_{1-x}N$/GaN layer 302 that is the GaN-based buffer layer. Here, the GaN-based single

crystalline layer 320 includes an undoped GaN layer 303, an Indium-doped GaN layer 304, and a silicon-doped n-GaN layer 306.

The $In_xGa_{1-x}N$/GaN layer 302 is grown with thickness less than 30 Å alternatively so that the GaN-based buffer layer having the superlattice structure is formed. The boundary defects caused by the differences between the thermal expansion coefficients of the GaN-based buffer layer and the substrate 301 and between the lattice constants of them are minimized so that good GaN-based nitride semiconductor can be obtained.

As shown in FIGs. 3(a) and 3(b), in the GaN-based single crystalline layer 320 laminated and formed on the $In_xGa_{1-x}N$/GaN layer 302 that is the GaN-based buffer layer, after the Indium-doped GaN layer 304 is formed, the undoped GaN layer 303 may be formed on the Indium-doped GaN layer 304. Otherwise, after the undoped GaN layer 303 is formed, the Indium-doped GaN layer 304 may be formed on the undoped GaN layer 303.

Since the nitride semiconductor having the above-mentioned structure is grown in the process similar to the fabrication method of the nitride semiconductor described in the first embodiment, the description of the fabrication method will be omitted.

Meanwhile, FIG. 4 is a cross-sectional view illustrating structure of a nitride semiconductor light emitting device fabricated in a nitride semiconductor fabrication method according to the present invention schematically.

The nitride semiconductor light emitting device according to the present invention includes a substrate 401, a GaN-based buffer layer 402 formed on the substrate 401, a first electrode layer of an n-GaN layer 405 formed on the GaN-based buffer layer 402; an activation layer

420 formed on the first electrode layer; and a second electrode layer of a p-GaN layer 410 formed on the activation layer 420.

Here, the GaN-based buffer layer 402 is formed in any one selected from a group consisting of a three-layered structure $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$, a two-layered structure $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$.

In other words, the nitride semiconductor light emission element according to the present invention is formed by growing a GaN-based nitride semiconductor as the GaN-based buffer layer 402 on a substrate (i.e. a sapphire substrate or a SiC substrate) 401, forming a silicon-doped n-GaN layer 405 as the first electrode layer, and forming a Mg-doped p-GaN layer 410 as the second electrode layer. The activation layer 420 of InGaN/GaN multiple quantum well structure is formed in a sandwich couple structure between the first electrode layer of the n-GaN layer 405 and the second electrode layer of the p-GaN layer 410.

Here, the activation layer 420 can consist of an $In_xGa_{1-x}N$ well layer 406, an $In_xGa_{1-x}N/GaN$ barrier layer 407, an $In_xGa_{1-x}N$ well layer 408 and an $In_xGa_{1-x}N/GaN$ barrier layer 409. The undoped GaN layer 403 or the Indium-doped GaN layer 404 may be formed between the GaN-based buffer layer 402 and the first electrode layer of the n-GaN layer 405.

Industrial Applicability

As described above, the nitride semiconductor and fabrication method thereof according to the present invention can reduce the crystal defects caused by a differences between thermal expansion coefficients of a

GaN-based single crystalline layer and a substrate and a difference between lattice constants of them and enhance the crystallinity of the GaN-based nitride semiconductor, to thereby improve the performance of the nitride semiconductor and assure reliability.

Claims

1. A nitride semiconductor comprising:

a substrate;

a GaN-based buffer layer formed on the substrate in any one selected from a group consisting of a three-layered structure $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$, a two-layered structure $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$; and

a GaN-based single crystalline layer formed on the GaN-based buffer layer.

2. The nitride semiconductor of claim 1, wherein the GaN-based single crystalline layer comprises:

an indium-doped GaN layer;

an undoped GaN layer formed on the Indium-doped GaN layer; and

a silicon-doped n-GaN layer formed on the undoped GaN layer.

3. The nitride semiconductor of claim 1, wherein the GaN-based single crystalline layer comprises:

an undoped GaN layer;

an indium-doped GaN layer formed on the undoped GaN layer; and

a silicon-doped n-GaN layer formed on the indium-doped GaN layer.

4. A nitride semiconductor light emitting device comprising:

a substrate;

a GaN-based buffer layer formed on the substrate in any one selected from a group consisting of a three-

layered structure $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$, a two-layered structure $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$;

a first electrode layer of an n-GaN layer formed on the GaN-based buffer layer;

an activation layer formed on the first electrode layer; and

a second electrode layer of a p-GaN layer formed on the activation layer.

5. The nitride semiconductor light emitting device of claim 4, further comprising:

an Indium-doped GaN layer formed on the GaN-based buffer layer; and

an undoped GaN layer formed on the Indium-doped GaN layer.

6. The nitride semiconductor light emitting device of claim 4, further comprising:

an undoped GaN layer formed on the GaN-based buffer layer; and

an Indium-doped GaN layer formed on the undoped GaN layer.

7. A method for fabricating a nitride semiconductor, the method comprising the steps of:

(a) growing a GaN-based buffer layer on a substrate in any one selected from a group consisting of a three-layered structure $Al_yIn_xGa_{1-x,y}N/In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$ and $0 \leq y \leq 1$, a two-layered structure $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$, and a superlattice structure of $In_xGa_{1-x}N/GaN$ where $0 \leq x \leq 1$; and

(b) growing a GaN-based single crystalline layer on the grown GaN-based buffer layer.

8. The method of claim 7, wherein the GaN-based buffer layer is grown in an MOCVD equipment at a temperature of 500 - 800 °C and in a thickness of 50 - 800 Å by introducing sources of TMGa, TMIn and TMAl and a gas of NH_3 at the same time while supplying carrier gases of H_2 and N_2.

9. The method of claim 8, wherein the GaN-based buffer layer is grown under a condition that flow of the sources of TMGa, TMIn and TMAl is 5 - 300 μmol/mim and growing pressure is 100 - 700 torr.

10. The method of claim 7, wherein the step (b) comprises the steps of:

growing an Indium-doped GaN layer;

growing an undoped GaN layer on the Indium-doped GaN layer; and

growing a silicon-doped n-GaN layer on the undoped GaN layer.

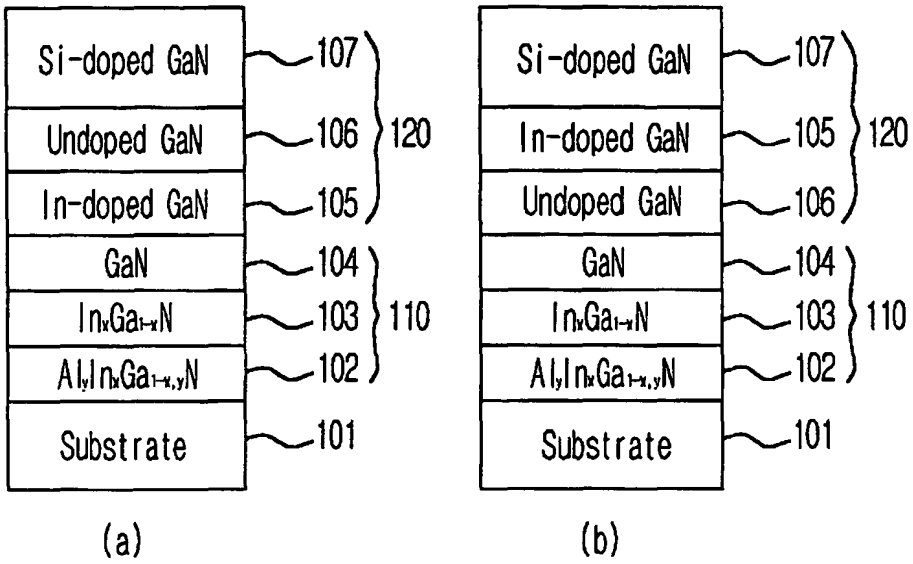
11. The method of claim 7, wherein the step (b) comprises the steps of:

growing an undoped GaN layer;

growing an Indium-doped GaN layer on the undoped GaN layer; and

growing a silicon-doped n-GaN layer on the Indium-doped GaN layer.

[FIG. 1]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107
Undoped GaN
106
120
In-doped GaN
105
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104
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102
Substrate
101
(a)
Si-doped GaN
107
In-doped GaN
105
120
Undoped GaN
106
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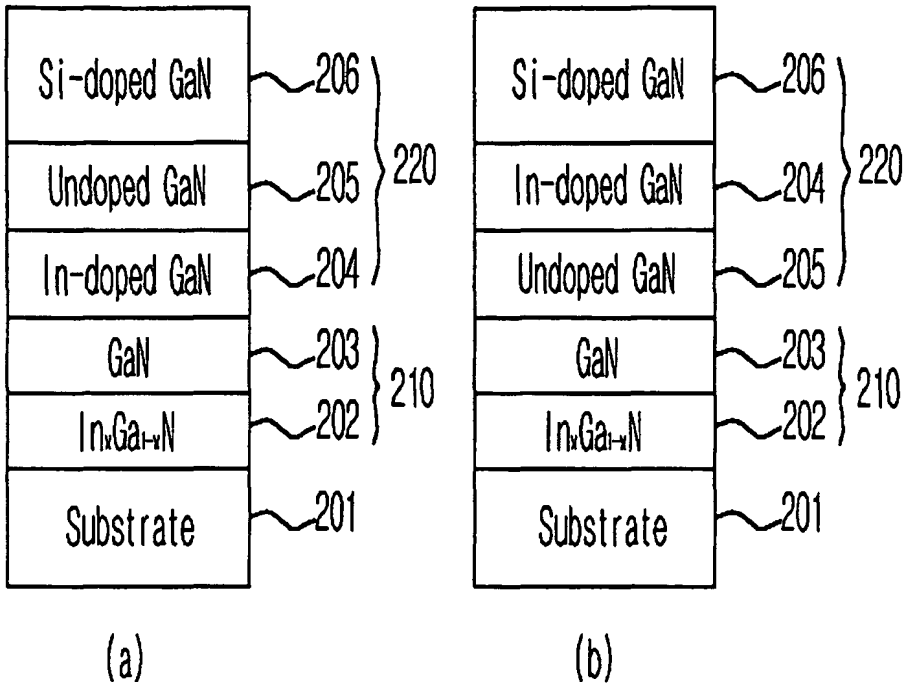
102
Substrate
101
(b)

[FIG. 2]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Undoped GaN
205
220
In-doped GaN
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GaN
203
210
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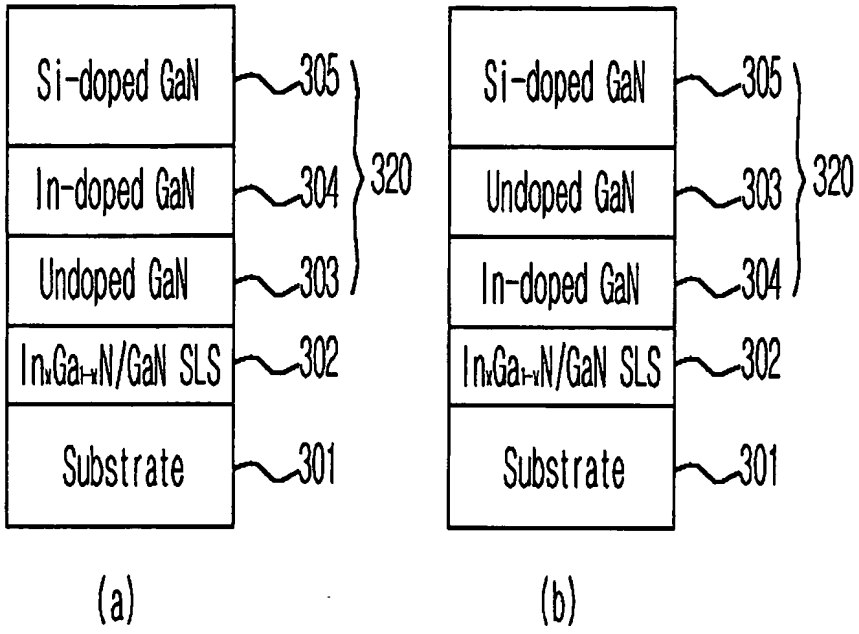
202
Substrate
201
(a)
Si-doped GaN
206
In-doped GaN
204
220
Undoped GaN
205
GaN
203
210
InxGa1-xN
202
Substrate
201
(b)

[FIG. 3]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In-doped GaN
304
320
Undoped GaN
303
InxGa1-xN/GaN SLS
302
Substrate
301
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Si-doped GaN
305
Undoped GaN
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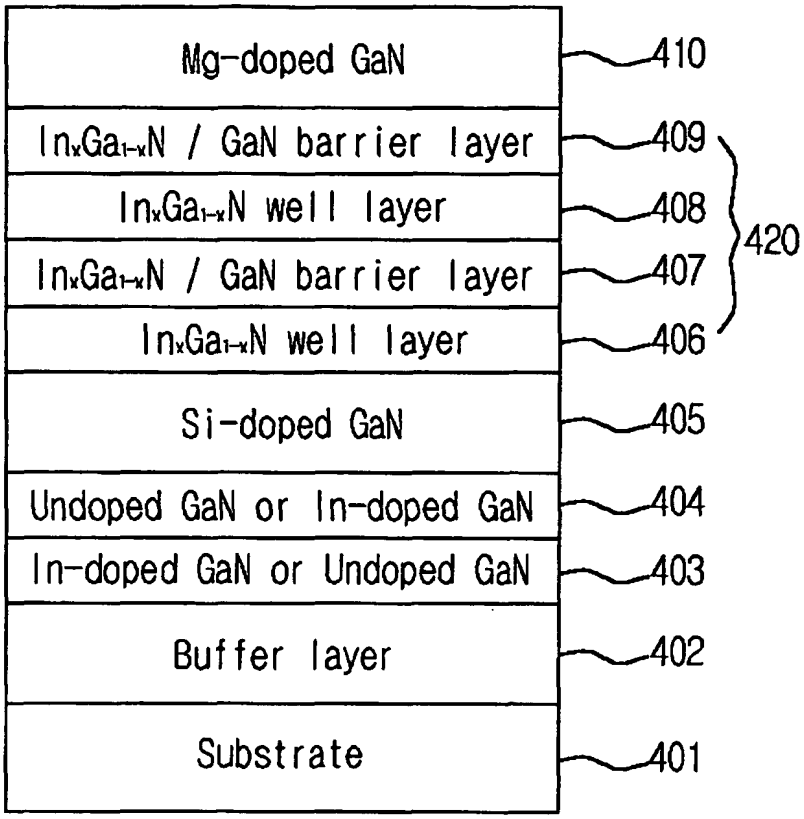
InxGa1-xN/GaN SLS
302
Substrate
301
(b)

[FIG. 4]


Mg-doped GaN
410
InxGa1-xN / GaN barrier layer
409
InxGa1-xN well layer
408
InxGa1-xN / GaN barrier layer
407
InxGa1-xN well layer
406
420
Si-doped GaN
405
Undoped GaN or In-doped GaN
404
In-doped GaN or Undoped GaN
403
Buffer layer
402
Substrate
401

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR03/01669

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H01L 33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L H01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean patents and applications for inventions, since 1975

Electronic data base consulted during the intertnational search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 10-173220 A2 (ROHM CO. LTD) 26 JUNE 1998 see the abstract, claim 1, paragraph [0010]-[0012], Figure 1	1, 4, 7, 8
A	see the whole documents	2-3, 5-6, 9-11
Y	JP 7-302929 A2 (SUMITOMO CHEM. CO. LTD) 14 NOVEMBER 1995 see the abstract, claim 1, embodiment 1, Figure 2	1, 4, 7, 8
A	see the whole documents	2-3, 5-6, 9-11
A	JP 2001-7397 A2 (NICHIA CHEM. IND. LTD) 12 JANUARY 2001 see the whole documents	1-11
A	JP 9-293897 A2 (ROHM CO. LTD) 11 NOVEMBER 1997 see the whole documents	1-11
A	JP 9-199759 A2 (TOYODA GOSEI CO. LTD, AKASAKI ISAMU, AMANO HIROSHI) 31 JULY 1997 see the whole documents	1-11

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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Date of the actual completion of the international search	Date of mailing of the international search report
24 NOVEMBER 2003 (24.11.2003)	24 NOVEMBER 2003 (24.11.2003)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR03/01669

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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JP 7-302929 A2	14.11.1995	NONE	
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JP 9-199759 A2	31.07.1997	NONE	